GENERAL INSTRUMENT	SP1000

PRELIMINARY INFORMATION

VOICE RECOGNITION/SYNTHESIS DEVICE

FEATURES

- N-channel silicon gate construction
- Single 5V supply
- On chip oscillator
- 0°C to +70°C operation
- User programable sample rate
- TTL compatible
- Standard microprocessor interface including 6809

RECOGNITION FEATURES

- Software controlled sampling frequency from 5.0kHz-15.9kHz
- Automatic gain control outputs for control of external input amplifier
- 8 stage Linear Predictive Coding (LPC) lattice analyzer

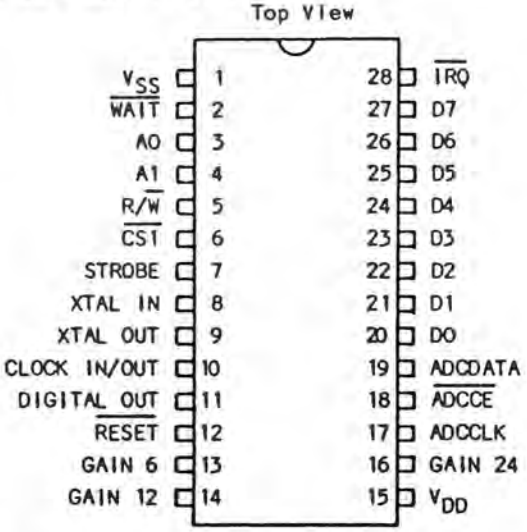
SYNTHESIZER FEATURES

- 10 stage lattice synthesizer
- Software controlled sampling frequency from 4.0kHz-12.7kHz
- Excitation look up ROM for voiced/unvoiced source
- 8 bit on chip digital to analog conversion with PWM digital output

PIN CONFIGURATION

28 LEAD DUAL IN LINE

Top View



DESCRIPTION

In voice recognition applications, the SP1000 forms the system front end by performing LPC feature extraction on an incoming audio signal. It must be supported by an 8 bit microcomputer which would compare the audio signal features with those of templates stored in memory, in order to make a recognition decision.

This results in a system design which leaves definition of key system features in the control of the system designer. Thus, this device can be used in speaker-dependent or speaker-independent systems, recognizing isolated words or connected speech.

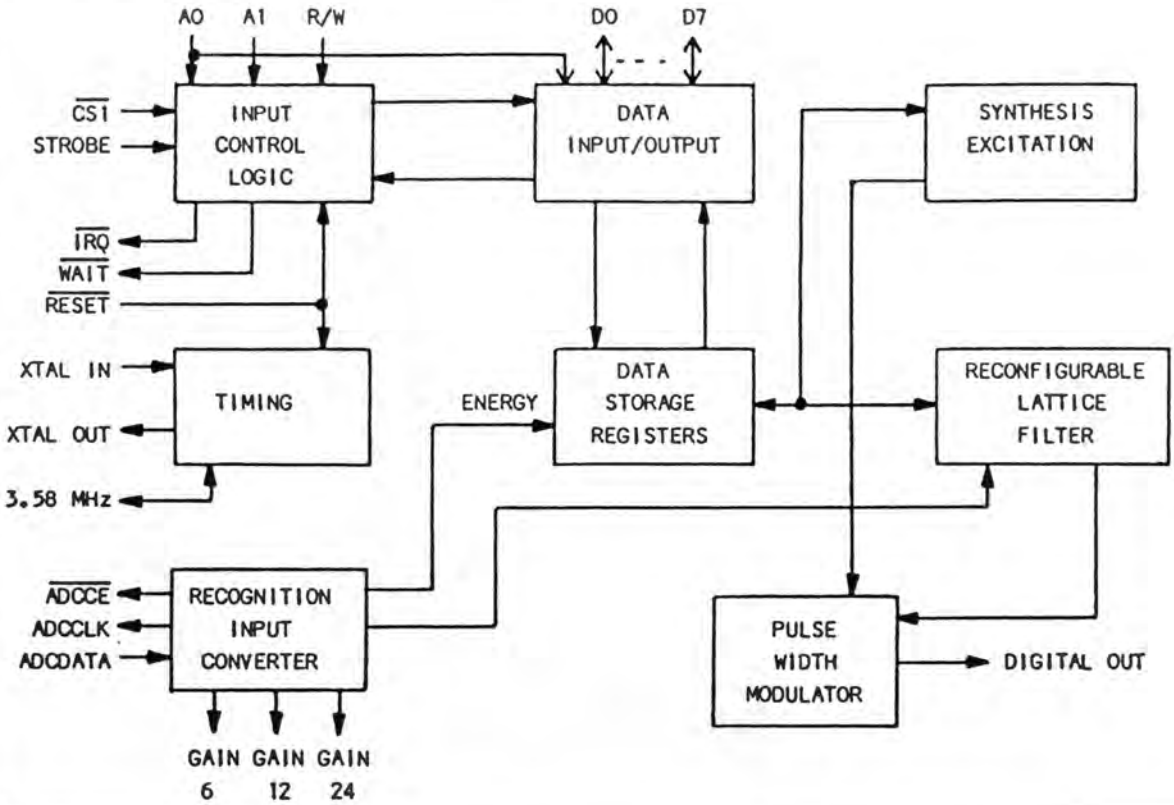
The advantage of this approach is that the designer is not locked-in to a recognition algorithm which may or may not suit the design requirements. In addition, since the recognition algorithm is contained in software or firmware it can be easily upgraded to take advantage of advances in recognition techniques, without requiring hardware redesign.

ARCHITECTURAL DESCRIPTION

Processor Interface:

The SP1000 Voice Recognition/Synthesis Device is designed to interface with a standard microprocessor bus, with data lines, address lines, chip select line, and read/write line. Eight bits of data may be read from, or written to the chip by

SP1000 BLOCK DIAGRAM



VOICE RECOGNITION/SYNTHESIS SYSTEM BLOCK DIAGRAM

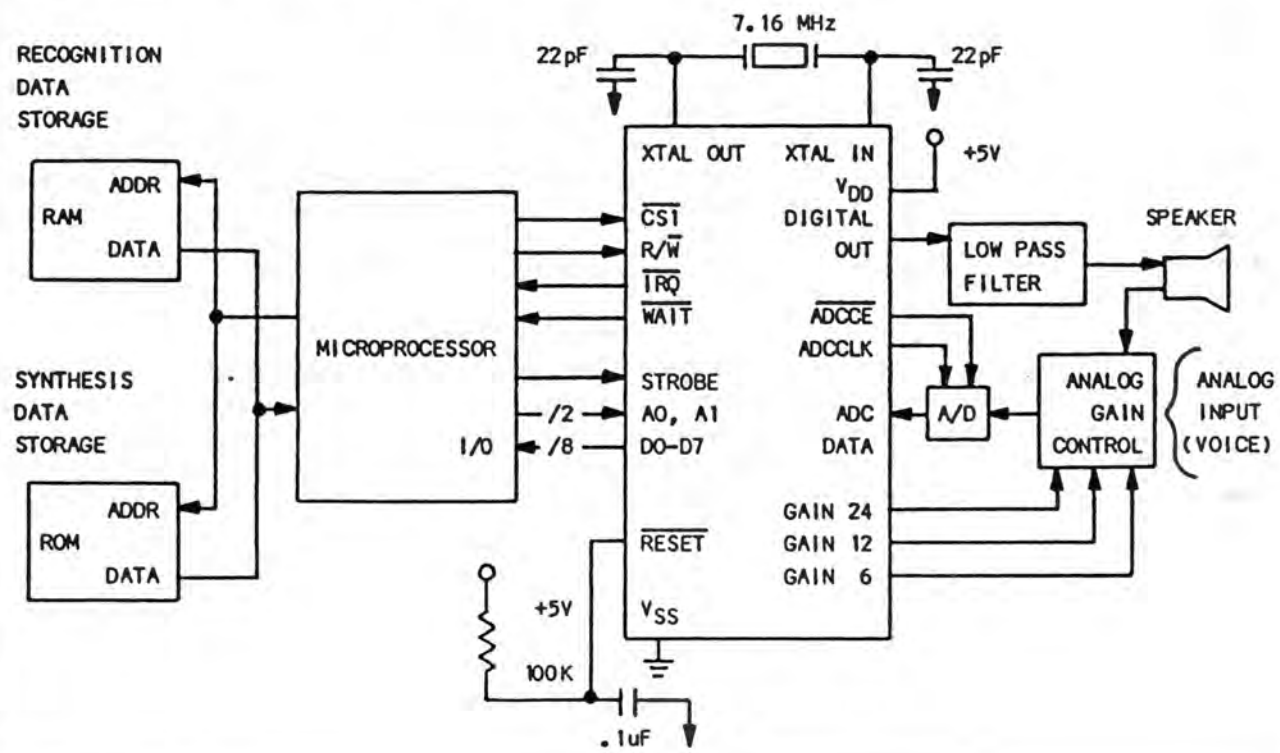


Table 1: OPERATION CODES

STROBE	$\overline{CS1}$	R/$\overline{W}$	A1	A0	Code	Operation
L	X	X	X	X		(Chip not selected)
X	H	X	X	X		
H	L	L	L	L	0	Write to Control Register
H	L	L	L	H	1	Write to Parameter Address Register
H	L	L	H	L	2	Write to Parameter Data Input Register, LSB = 0
H	L	L	H	H	3	Write to Parameter Data Input Register, LSB = 1
H	L	H	L	L	4	Read Status Register
H	L	H	L	H	5	(Not Implemented)
H	L	H	H	L	6	Read Parameter Data Output Register
H	L	H	H	H	7	Same as Code 6, plus Initiate Internal Fetch

the processor, following standard peripheral protocol. A nine-bit word may be written to the chip during a coefficient write. Data is transferred via the data lines whenever the chip select line is active. The read/write line determines the direction of the transfer, and the address lines specify a particular register within the chip as source or destination. Another way of looking at the address lines is that they define, together with the read/write line (R/$\overline{W}$), a particular operation to be performed. Table 1 presents the available defined operations. The code column will be used for reference, e.g. the operation of writing to the Parameter Address Register will be referred to as a Code 1 operation.

Before describing the operations in detail, the data organization inside the device will be reviewed. There is a sharp distinction between control/status information and parameter data. Parameter data inside the chip resides in two large recirculating shift registers. The recirculation period is the same as the sample period. Access to a particular parameter can occur only once each recirculation period, when that parameter is passing by a fixed point of access. The access is bit serial, and the processor cannot access parameter data directly. One of the functional blocks inside the chip is a special interface to overcome this problem.

The interface bears some analogy to a serial communication channel for simplex mode operation. Parameter data written by the processor is first stored in the Parameter Data Input Register. A BUSY flag is set to indicate that the register is full. The contents of the Parameter Data Input Register will be written to the destination specified by the Parameter Address Register as soon as that destination becomes accessible. Upon completion, the BUSY flag is reset to signal the processor that the Parameter Data Input Register is empty and ready for another data transfer.

For the processor to read a parameter value, the interface must first perform a fetch operation. The fetch operation is initiated by the processor. The BUSY flag is set to indicate fetch in progress. As soon as the parameter (specified by the Parameter Address Register) becomes accessible, the value (truncated to eight bits if necessary) is transferred to the Parameter Data Output Register, and the BUSY flag is reset. The processor can now read the parameter value from the Parameter Data Output Register.

The reading and writing of parameter data requires a finite amount of time. During that time the interface cannot be disturbed. The processor, therefore, must monitor the state of the BUSY flag in all dealings with the device. The BUSY flag is reflected in the STATUS Register.

PIN FUNCTIONS

Pin Number	Name	Function
1	V_{SS}	Ground
2	$\overline{WAIT}$	This output pin is normally high, but is taken low if the chip is selected for code 1, 2, 3, or 7 operation while the BUSY flag is set. It remains low until the BUSY flag is reset, or the chip is de-selected. This is an open drain output.
3	A_0	Least significant address line/ninth data line. (Least Significant Bit, input only.)
4	A_1	Most significant address line.
5	R/W	Read/Write. The state of input Pins 3, 4, and 5 determines the operation to be performed, according to Table 1.
6, 7	$\overline{CS1}$, STROBE	Chip select inputs: $\overline{CS1}$ active low, STROBE active high. Both must be active to select the chip.
8	XTAL IN	Crystal In. Input connection for a 7.16 MHz crystal.
9	XTAL OUT	Crystal Out. Output connection for a 7.16 MHz crystal.
10	CLOCK IN/OUT	3.58 MHz test Clock Input/buffered Clock Output. As an input, it allows the chip to be driven by an external clock (one-half the crystal frequency), in which case the crystal oscillator is disabled. As an output, it provides the buffered system clock which is one half of the crystal frequency.
11	DIGITAL OUT	Synthesized speech Digital Output. This is the output of the Pulse Width Modulator (PWM). The PWM, in conjunction with an external low pass filter, forms a digital to analog converter with eight bits of resolution.
12	$\overline{RESET}$	A logic 0 resets the chip. It must be returned to a logic 1 for normal operation.
13, 14, 16	GAIN 6, GAIN 12, GAIN 24	These 3 outputs can control 3 analog switches. The switches determine the gain of the external amplifier which precedes the analog to digital converter.
15	V_{DD}	Power supply pin.

PIN FUNCTIONS (continued)

Pin Number	Name	Function
17	ADCCLK	ADC Clock. This output is the 150kHz gated clock. It is active only while $\overline{ADCCE}$ is active, otherwise it is held low.
18	$\overline{ADCCE}$	ADC Chip Enable. This output provides chip select for the analog to digital converter. It also controls the sample and hold circuit.
19	ADCDATA	ADC Data In. This input pin receives the serial data from the analog to digital converter.
20-27	D0-D7	Data lines. These 8 pins are the bi-directional data bus for connection to the processor. D7 carries the most significant bit.
28	$\overline{IRQ}$	Interrupt Request. This active-low output provides interrupt of the processor. This pin is an open drain output.

PARAMETER DESCRIPTION

Following is a short description of the parameters as listed in Table 2.

Synthesis

K_{10}-K_1:
These are the ten lattice filter coefficients for synthesis mode. Using the least significant address line as the ninth data line allows these to be specified with nine bits of resolution. K_{10} is the coefficient associated with the first filter section (closest to the excitation).

EXCTYP:
This eight-bit wide field is split in half to contain two parameters; Post Filter Gain and Excitation Type.

a) Post Filter Gain
The three least significant bits determine the post filter gain by determining which consecutive eight bits from the nominal sixteen-bit output of the filter will be sent to the digital to analog converter. A code of zero will choose the eight most significant bits (with proper sign extend) of the filter output. An increase of one will push the choice one bit to the right, such that a code of seven will choose the eight bits following the three most significant bits of the filter output.

Table 2: PARAMETER ADDRESS REGISTER

MSB 7	6	5	4	3	2	1	LSB 0
NOT USED		COEF BUF	NOT USED	INDEX			

Bits 0-3 Specify Parameter Index
Bit 5 Specifies Buffer (=1 for SR in recognition mode; otherwise = 0)

	Index	Parameter	
		Synthesis	Recognition
BIT 5 = 0	0	K_{10}	K_{R1}
	1	K_9	K_{R2}
	2	K_8	K_{R3}
	3	K_7	K_{R4}
	4	K_6	K_{R5}
	5	K_5	K_{R6}
	6	K_4	K_{R7}
	7	K_3	K_{R8}
	8	K_2	ENRGY
	9	K_1	T1
	A	EXCTYP	T2
	B	EXCAMP	SR
	C	T1	-
	D	T2	-
	E	SR	-
	F	-	-
BIT 5 = 1	B	-	SR

EXCAMP:
This field controls the amplitude of the selected excitation wave form. It is a gain factor specified as a base 2 logarithm, which is applied to each sample of the internally generated excitation. A special case exists when the excitation type is 1. The internally generated excitation is now a constant value. By writing a new value to the EXCAMP field every sample period, the constant value is modulated and externally generated excitation of the synthesizer is achieved. The gain factor is expressed in two parts: the most significant bit gives the sign of the gain factor (it is actually needed only for externally specified excitation); the seven least significant bits are the base 2 logarithm of its magnitude. These seven bits are interpreted as four exponent bits and three mantissa bits.

The reading of a particular, randomly selected parameter requires the following steps:

1. Load the Parameter Address Register by executing a write instruction, Operation Code 1. (See Table 1.)

2. Initiate a fetch operation (internal to the chip), by executing a read instruction with Operation Code 7. This will cause the BUSY flag (bit 7 of the STATUS Register) to become set. The fact that a read instruction is used will cause the current contents of the Parameter Data Output Register to be overwritten.

3. Wait for the BUSY flag to become reset, signaling the completion of the fetch sequence. The STATUS Register is read by a read instruction, Operation Code 4.

4. Read the desired parameter value by executing a read instruction, Operation Code 6.

Upon completion of a fetch (or store) operation, the Parameter Address Register is automatically updated to specify the next parameter in sequence. The sequence for synthesis is: K_{10}, $K_9 \ldots K_1$, EXCTYP, EXCAMP, T1, T2, SR. For recognition the sequence is K_{R1}, $K_{R2} \ldots K_{R8}$, ENRGY, T1, T2, SR. This automatic update simplifies sequential reading of parameters. Sequential reading of parameters requires the following steps:

1. Load the address of the first parameter to be read, as in step 1, above.

2. Initiate the first fetch operation, as in step 2, above.

3. Wait for the BUSY flag to become reset, as in step 3, above.

4. Execute a read instruction with Operation Code 7. This will read the parameter value and also initiate the fetch of the next parameter in the sequence.

5. Go to step 3.

Synthesis and Recognition

T1 and T2:
These two identical fields control the two programable timers. The timers are actually sample time counters, and the fields contain the value to be counted down for each.

SR (Sample Rate):
The low order six bits of this field indirectly determine the Sample Rate by specifying how many clock cycles of dead time should be inserted between the processing of each filter stage. The formula for Sample Rate is:

$$f_s = f_c / [(28+n) * m] \quad \text{where}$$

f_s is Sample Rate.
f_c is system clock rate (3.579545 MHz).
n is the integer represented by the six low order bits of the SR field.
m is the number of filter stages, 10 for synthesis and 8 for recognition.

The two most significant bits of the field are used for a different parameter pertaining to recognition only.

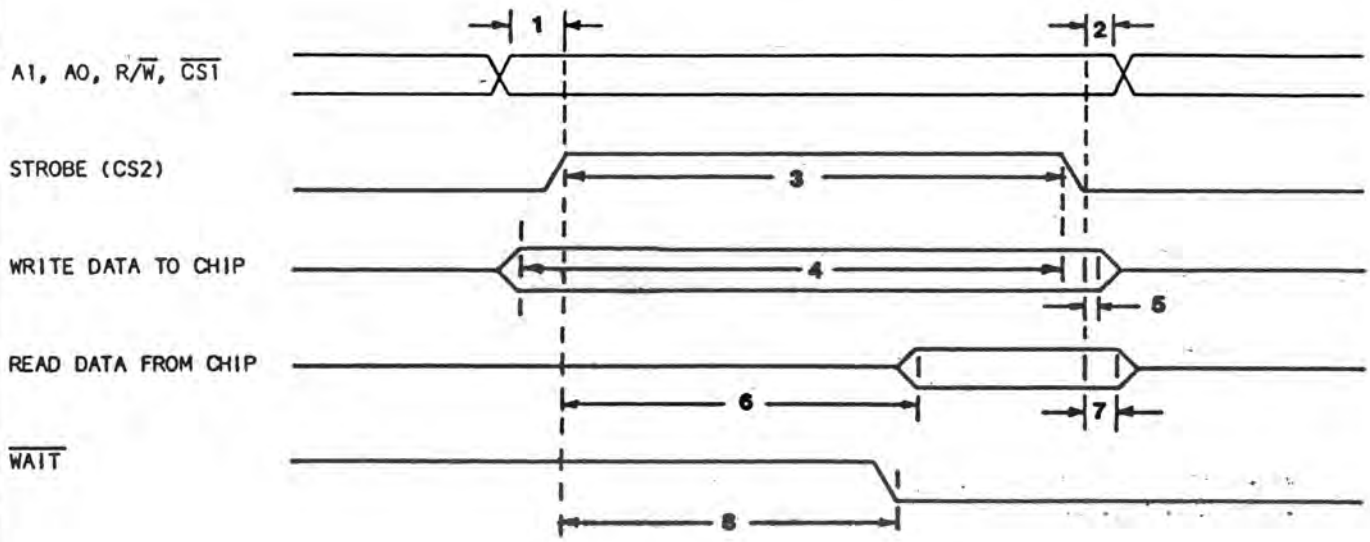
Recognition

K_{R1}-K_{R8}:
These are eight bit coefficients produced by the adaptive lattice filter in recognition mode. Two different representations of these are available to the processor. Averaged values are read from the first circular buffer (BUF=0 in the Parameter Address Register) and instantaneous values may be read from the other buffer (BUF=1).

ENRGY:
This eight bit field contains information generated by the chip. It is a measure of the magnitude of incoming speech samples averaged over time, and is expressed on a logarithmic scale.

SR (two high order bits only)
This 2-bit field specifies the set point for gain control.

PROCESSOR BUS TIMING



	MIN	MAX
1. Address Set Up Time	70ns	-
2. Address Hold Time	20ns	-
3. Strobe Pulse Width	210ns	-
4. Write Data Set Up	280ns	-
5. Write Data Hold	30ns	-
6. Read Data Access		220ns
7. Read Data Hold	10ns	
8. WAIT Access		140ns

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD}..... -0.3V to +8V
Storage Temperature..... -25°C to +125°C

Clock

Crystal Frequency..... 7.15909 MHz
Standard Conditions (unless otherwise stated)
Clock In (Optional)..... 3.579545 MHz

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C
Standard Conditions (unless otherwise stated)
V_{DD} = 5V ± 5%
V_{SS} = GND

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied - operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics	Sym	Min	Max	Units	Conditions
DC Characteristics					
Supply Voltage	V_{DD}	4.5	5.5	V	
Supply Current	I_{DD}	-	100	mA	25°C, No output loads.
Inputs (ADCDATA, STROBE, $\overline{CS1}$, R/$\overline{W}$, A1, A0, $\overline{RESET}$)					
Input Logic 0	V_{IL}	0.0	0.8	V	
Input Logic 1	V_{IH}	2.0	V_{DD}	V	
Input Leakage	I_L	-	10	µA	V_{PIN} = 5.5V and 0.0V V_{DD} = 5.5V V_{SS} = 0.0V
Input/Outputs (D0-D7 CLOCK I/O)					
Input Logic 0	V_{IL}	0.0	0.8	V	
Input Logic 1	V_{IH}	2.0	V_{DD}	V	
Output Logic 0	V_{OL}	-	0.6	V	I_{OL} = 1.60 mA 50pf (4 LS TTL Loads)
Output Logic 1	V_{OH}	2.4	-	V	I_{OH} = 100 uA
Output Leakage	I_L	-	10	µA	V_{PIN} = 5.5V and 0.0V V_{DD}, CS1 = 5.5V V_{SS} = 0.0V
Open Drain Outputs (IRQ, MRDY)					
Output Logic 0	V_{OL}	-	0.6	V	I_{OL} = 1.60mA 50pf (4 LS TTL Loads)
Output Leakage	I_L	-	10	µA	V_{PIN} = 5.5V and 0.0V V_{DD} = 5.5V V_{SS} = 0.0V
Outputs (DIGITAL OUT, GAIN 6, 12, 24, ADCCLK, $\overline{ADCCE}$)					
Output Logic 0	V_{OL}	-	0.6	V	I_{OL} = 1.60mA 50pf
Output Logic 1	V_{OH}	2.4	-	V	(4LS TTL Loads) I_{OH} = -100 µA

REGISTERS

CONTROL REGISTER:

MSB 7	6	5	4	3	2	1	LSB 0
NU	SYN/ REC	ENB T1	ENB T2	ADD/ REPL	TIMER 1 TIMER 2	TEST 2	TEST 1

Bit 7 - NU — Not Used

6 - SYN/$\overline{REC}$ — 1 = Synthesis, 0 = Recognition

5 - ENB T1 — Set to One to Enable Timer 1 Interrupt to IRQ pin 28

4 - ENB T2 — Set to One to Enable Timer 2 Interrupt to IRQ pin 28

3 - ADD/$\overline{REPL}$ — 1 = Add to, 0 = Replace Parameter Value in First Buffer ((BUF) = 0)

2 - TIMER 1 — 1 = Timer 1, 0 = Timer 2, Causing Implementation of New Parameter Set

1 - TEST INTERNAL DATA — 1 = Test Mode. Internal data on Pin 11
0 = Normal Mode. D/A PWM on Pin 11

0 - TEST EXTERNAL CLOCK — 1 = Test Mode. Oscillator not used. Pin 10 is input. Use 3.58MHz
0 = Normal Mode. Pin 10 is output of 3.58MHz. lator is used.

STATUS REGISTER:

MSB 7	6	5	4	3	2	1	LSB 0
BUSY	S/R	T1	T2	COINC	NU	NU	NU

Bit 7 - BUSY — Processor Interface Busy

6 - S/$\overline{R}$ — High for Synthesis, Low for Recognition

5 - T1 OUT — Timer 1: Time-Out Flag (Latched)* (See note 1)

4 - T2 OUT — Timer 2: Time-Out Flag (Latched)* (See note 1)

3 - COINC — Current Slot Number Equals Parameter Address Register Slot Number

2 - NU — Not Used

1 - NU — Not Used

0 - NU — Not Used

Note 1:
*The timer flags are cleared by trailing edge of READ STATUS command.

PARAMETER ADDRESS REGISTER:

MSB 7	6	5	4	3	2	1	LSB 0
NOT USED		COEF BUF	NOT USED	INDEX			

Bits 0-3 — Specify Parameter

Bit 5 — Specifies Buffer

Bits 4, 6, 7 — Not Used